

Generic 24-Pin PAL® Device
Features

- Ultra high speed supports today's and tomorrow's fastest microprocessors
 - $t_{PD} = 7.5 \text{ ns}$
 - $t_{SU} = 3 \text{ ns}$
 - $f_{MAX} = 105 \text{ MHz}$
- Reduced ground bounce and under-shoot
- PLCC and LCC packages with additional V_{CC} and V_{SS} pins for lowest ground bounce
- Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8
- Up to 22 inputs and 10 outputs for more logic power

- 10 user-programmable output macrocells
 - Output polarity control
 - Registered or combinational operation
 - Pin or product term output enable control
- Preload capability for flexible design and testability
- High reliability
 - Proven Ti-W fuse technology
 - AC and DC tested at the factory
- Security Fuse

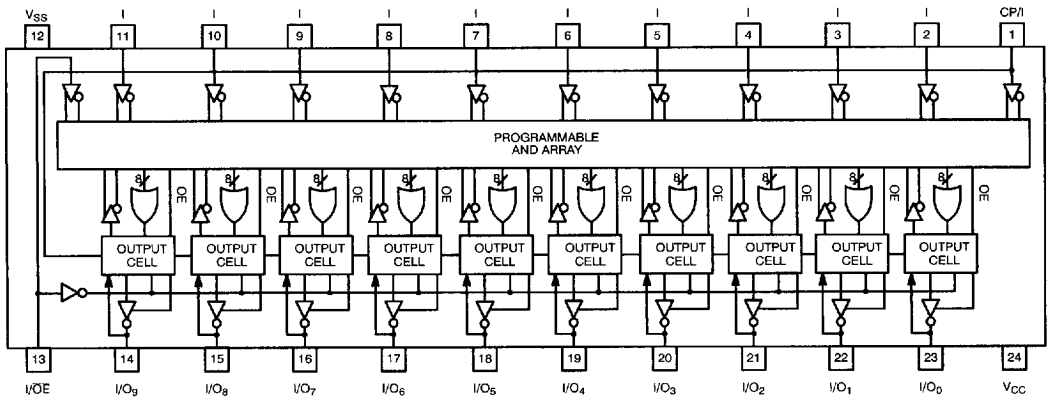
Functional Description

The PLD20G10C is a generic 24-pin device that can be used in place of 24 PAL devices. Thus, the PLD20G10C provides significant design, inventory, and programming flexibility over dedicated 24-pin devices.

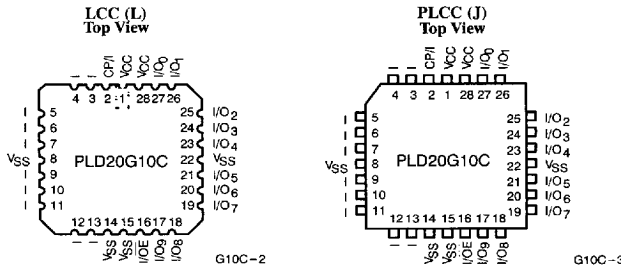
Using BiCMOS process and Ti-W fuses, the PLD20G10C implements the familiar sum-of-products (AND-OR) logic structure. It provides 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O or a common pin controlled \overline{OE} function allows this selection.

The PLD20G10C automatically resets on power-up. The Q output of all internal registers is set to a logic LOW and the \overline{Q} output to a logic HIGH. In addition, the PRELOAD capability allows the registers to be set to any desired state during testing.

A security fuse is provided to prevent copying of the device fuse pattern.

Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration


G10C-1

Pin Configurations


G10C-2

G10C-3

PAL is a registered trademark of Advanced Micro Devices

Selection Guide

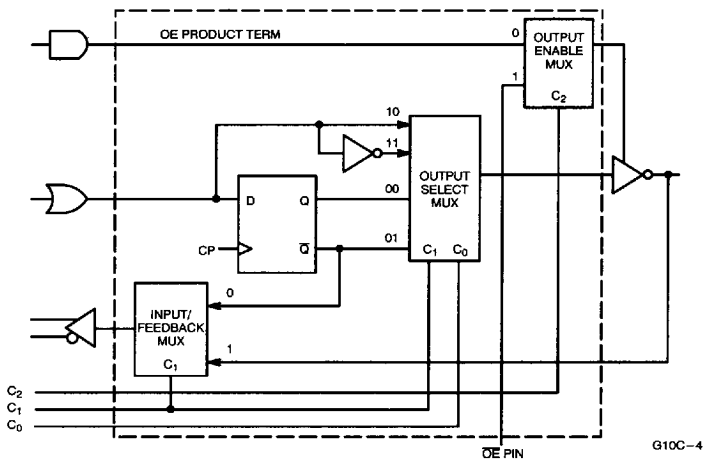
		20G10C-7	20G10C-10	20G10C-12	20G10C-15
I_{CC} (mA)	Commercial	190	190	190	
	Military		190	190	190
t_{PD} (ns)	Commercial	7.5	10	12	
	Military		10	12	15
t_s (ns)	Commercial	3.0	3.6	4.5	
	Military		3.6	4.5	7.5
t_{CO} (ns)	Commercial	6.5	7.5	9.5	
	Military		7.5	9.5	10
f_{MAX} (MHz)	Commercial	105	90	71	
	Military		90	71	57

Programmable Macrocell

The PLD20G10C has 10 programmable I/O macrocells (see Macrocell). Two fuses (C_1 and C_0) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output. An additional fuse (C_2) determines the source of the output enable signal. The signal can be generated either from the individual OE product term or from a common external OE pin.

Programming

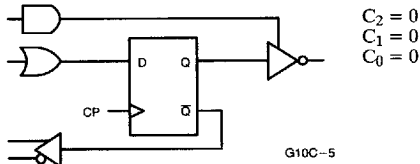
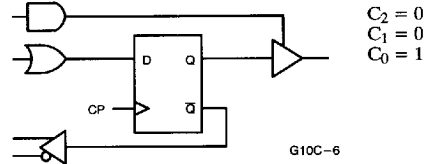
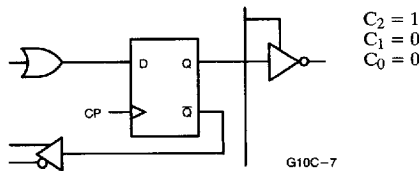
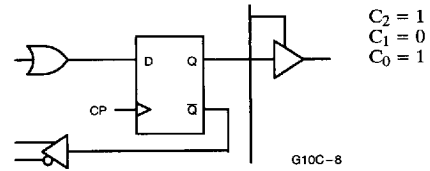
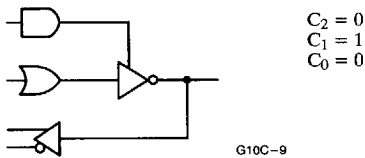
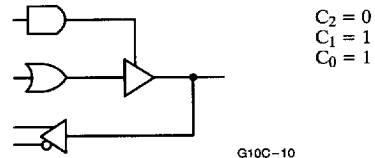
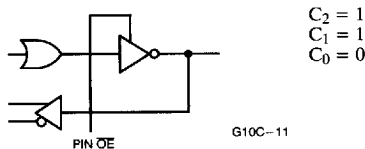
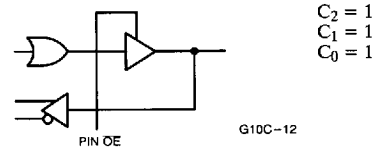
The PLD20G10C can be programmed using the *Impulse3™* programmer available from Cypress Semiconductor. See third party information is Cypress's Third Party Tools datasheet for further information.

Macrocell


Impulse3 is a trademark of Cypress Semiconductor Corporation.

Configuration Table

Figure	C ₂	C ₁	C ₀	Configuration
1	0	0	0	Product Term OE/Registered/Active LOW
2	0	0	1	Product Term OE/Registered/Active HIGH
5	0	1	0	Product Term OE/Combinatorial/Active LOW
6	0	1	1	Product Term OE/Combinatorial/Active HIGH
3	1	0	0	Pin $\overline{\text{OE}}$ /Registered/Active LOW
4	1	0	1	Pin $\overline{\text{OE}}$ /Registered/Active HIGH
7	1	1	0	Pin $\overline{\text{OE}}$ /Combinatorial/Active LOW
8	1	1	1	Pin $\overline{\text{OE}}$ /Combinatorial/Active HIGH

Registered Output Configurations

Figure 1. Product Term OE/Active LOW

Figure 2. Product Term OE/Active HIGH

Figure 3. Pin $\overline{\text{OE}}$ /Active LOW

Figure 4. Pin $\overline{\text{OE}}$ /Active HIGH
Combinatorial Output Configurations^[1]

Figure 5. Product Term OE/Active LOW

Figure 6. Product Term OE/Active HIGH

Figure 7. Pin $\overline{\text{OE}}$ /Active LOW

Figure 8. Pin $\overline{\text{OE}}$ /Active HIGH
Note:

1. Bidirectional I/O configurations are possible only when the combinatorial output option is selected.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential -0.5V to +7.0V
 DC Voltage Applied to Outputs in High Z State -0.5V to V_{CC}
 DC Input Voltage -0.5V to V_{CC}

DC Input Current - 30 mA to +5 mA (except during programming)
 DC Program Voltage 10V

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 5%
Military ^[2]	-55°C to +125°C	4.75V to 5.5V

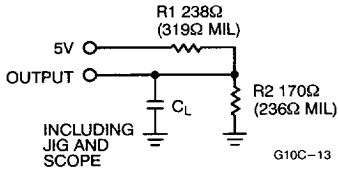
DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.2 mA	Com'l	2.4	
			I _{OH} = -2 mA	Mil		
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 16 mA	Com'l		0.5
			I _{OL} = 12 mA	Mil		
V _{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs ^[3]		2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs ^[3]			0.8	V
I _{IX}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ 2.7V, V _{CC} = Max.		-250	50	μA
I _I	Maximum Input Current	V _{IN} = V _{CC} , V _{CC} = Max.	Com'l		100	μA
			Mil		250	
I _{OZ}	Output Leakage Current	V _{CC} = Max., V _{SS} ≤ V _{OUT} ≤ V _{CC}		-100	100	μA
I _{SC}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.5V ^[4]		-30	-120	mA
I _{CC}	Power Supply Current	V _{CC} = Max., V _{IN} = GND, Outputs Open	Com'l		190	mA
			Mil		190	

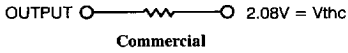
Capacitance^[5]

Parameter	Description	Max.	Unit
C _{IN}	Input Capacitance	8	pF
C _{OUT}	Output Capacitance	10	pF

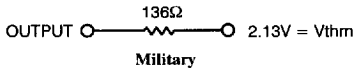
- Notes:
- T_A is the "instant on" case temperature.
 - These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
 - Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
 - Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


C_L ^[6]	Package
15 pF	P/D
50 pF	J/K/L

 Equivalent to: THÉVENIN EQUIVALENT
 99Ω


Equivalent to: THÉVENIN EQUIVALENT



Parameter	V_{th}	Output Waveform—Measurement Level
$t_{ER}(-), t_{PHZ}$	1.5V	
$t_{ER}(+), t_{PLZ}$	2.6V	
$t_{EA}(+), t_{PZH}$	1.5V	
$t_{EA}(-), t_{PZL}$	1.5V	

Note:

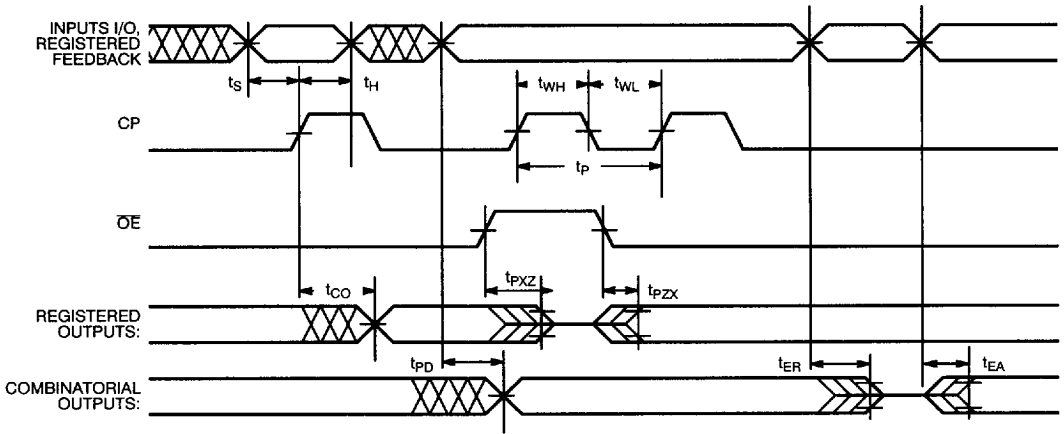
 6. $C_L = 5$ pF for t_{ER} and t_{PZ} measurements for all packages.

Switching Characteristics PLD20G10C⁽⁷⁾

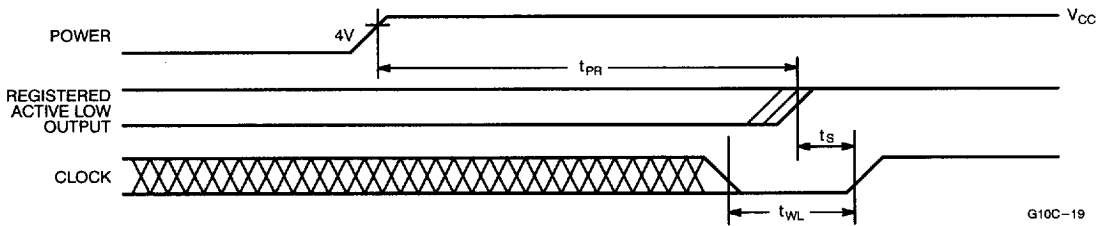
Parameter	Description	20G10C-7		20G10C-10		20G10C-12		20G10C-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{PD}	Input to Output Propagation Delay ^[8]	2	7.5	2	10	2	12	2	15	ns
t _{EA}	Input to Output Enable Delay	2	7.5	2	10	2	12	2	15	ns
t _{ER}	Input to Output Disable Delay ^[9]	2	7.5	2	10	2	12	2	15	ns
t _{PZX}	\overline{OE} Input to Output Enable Delay	2	7.5	2	10	2	12	2	15	ns
t _{PXZ}	\overline{OE} Input to Output Disable Delay	2	7.5	2	10	2	12	2	15	ns
t _{CO}	Clock to Output Delay ^[8]	1	6.5	1	7.5	1	9.5	1	10	ns
t _S	Input or Feedback Set-Up Time	3		3.6		4.5		7.5		ns
t _H	Input Hold Time	0		0		0		0		ns
t _P	External Clock Period (t _{CO} + t _S)	9		11.1		14		17.5		ns
t _{WH}	Clock Width HIGH ^[5]	3		3		3		6		ns
t _{WL}	Clock Width LOW ^[5]	3		3		3		6		ns
f _{MAX1}	External Maximum Frequency (1/(t _{CO} + t _S)) ^[10]	105		90		71		57		MHz
f _{MAX2}	Data Path Maximum Frequency (1/(t _{WH} + t _{WL})) ^[5, 11]	166		166		166		83		MHz
f _{MAX3}	Internal Feedback Maximum Frequency (1/(t _{CF} + t _S)) ^[12]	133		100		83		66		MHz
t _{CF}	Register Clock to Feedback Input ^[13]		4.5		6.4		7.5		7.5	ns
t _{PR}	Power-Up Reset Time ^[14]	1		1		1		1		μs

Notes:

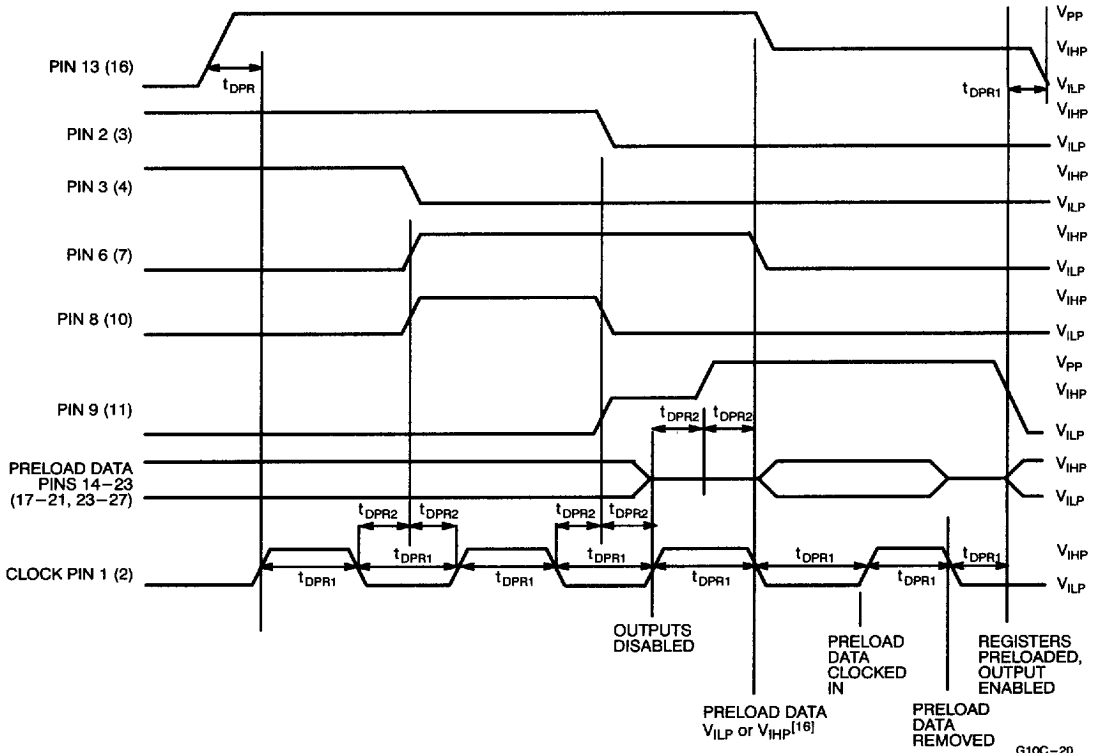
7. AC test load used for all parameters except where noted.
8. This specification is guaranteed for all device outputs changing state in a given access cycle.
9. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
13. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 12) minus t_S.
14. The registers in the PLD20G10C have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

Switching Waveform


G10C-18

Power-Up Reset Waveform^[14]


G10C-19

Preload Waveform^[15]


G10C-20

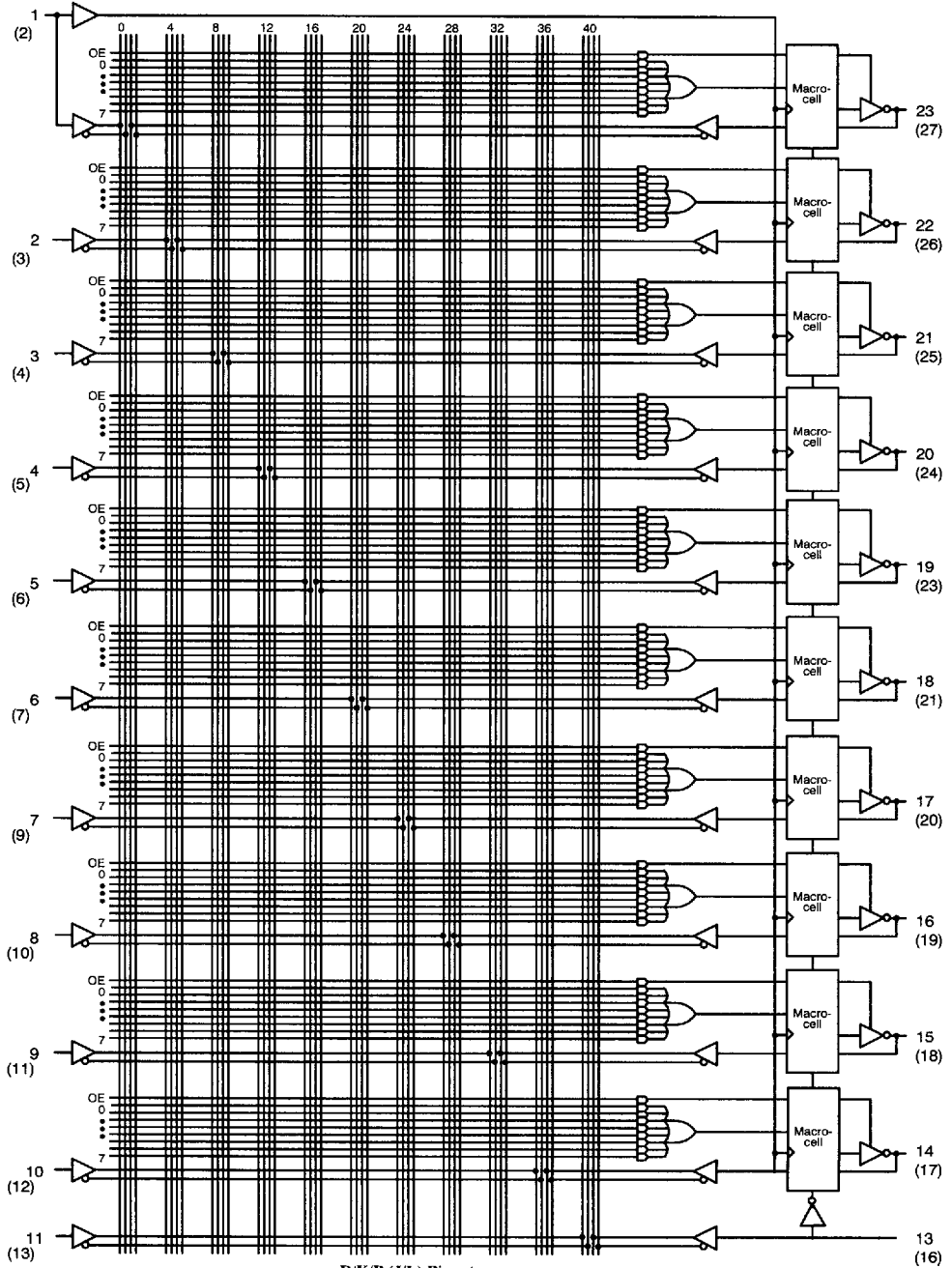
Notes:

15. Pins 4 (5), 5 (6), 7 (9) at V_{ILP} ; Pins 10 (12) and 11 (13) at V_{IHP} ; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}
16. Pins 2-8 (3-7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

D/K/P (J/L) Pinouts

Forced level on register pin during preload	Register Q output state after preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		μs
t_{DPR2}	Delay for Preload	0.5		μs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V
V_{CCP}	V_{CC} for Preload	4.75	5.25	V

Functional Logic Diagram for PLD20G10C


D/K/P (J/L) Pinouts

2-55

G10C-21

■ 2589662 0012956 598 ■

2

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
190	7.5	105	PLD20G10C-7DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PLD20G10C-7JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PLD20G10C-7PC	P13	24-Lead (300-Mil) Molded DIP	
	10	90	PLD20G10C-10DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PLD20G10C-10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PLD20G10C-10PC	P13	24-Lead (300-Mil) Molded DIP	
			PLD20G10C-10DMB	D14	24-Lead (300-Mil) CerDIP	Military
			PLD20G10C-10KMB	K73	24-Lead Rectangular Cerpack	
			PLD20G10C-10LMB	L64	28-Square Leadless Chip Carrier	
	12	71	PLD20G10C-12DC	D14	24-Lead (300-Mil) CerDIP	Commercial
			PLD20G10C-12JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PLD20G10C-12PC	P13	24-Lead (300-Mil) Molded DIP	
PLD20G10C-12DMB			D14	24-Lead (300-Mil) CerDIP	Military	
PLD20G10C-12KMB			K73	24-Lead Rectangular Cerpack		
PLD20G10C-12LMB			L64	28-Square Leadless Chip Carrier		
15	57	PLD20G10C-15DMB	D14	24-Lead (300-Mil) CerDIP	Military	
		PLD20G10C-15KMB	K73	24-Lead Rectangular Cerpack		
		PLD20G10C-15LMB	L64	28-Square Leadless Chip Carrier		

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

Document #: 38-A-00027-A